

### Product Features

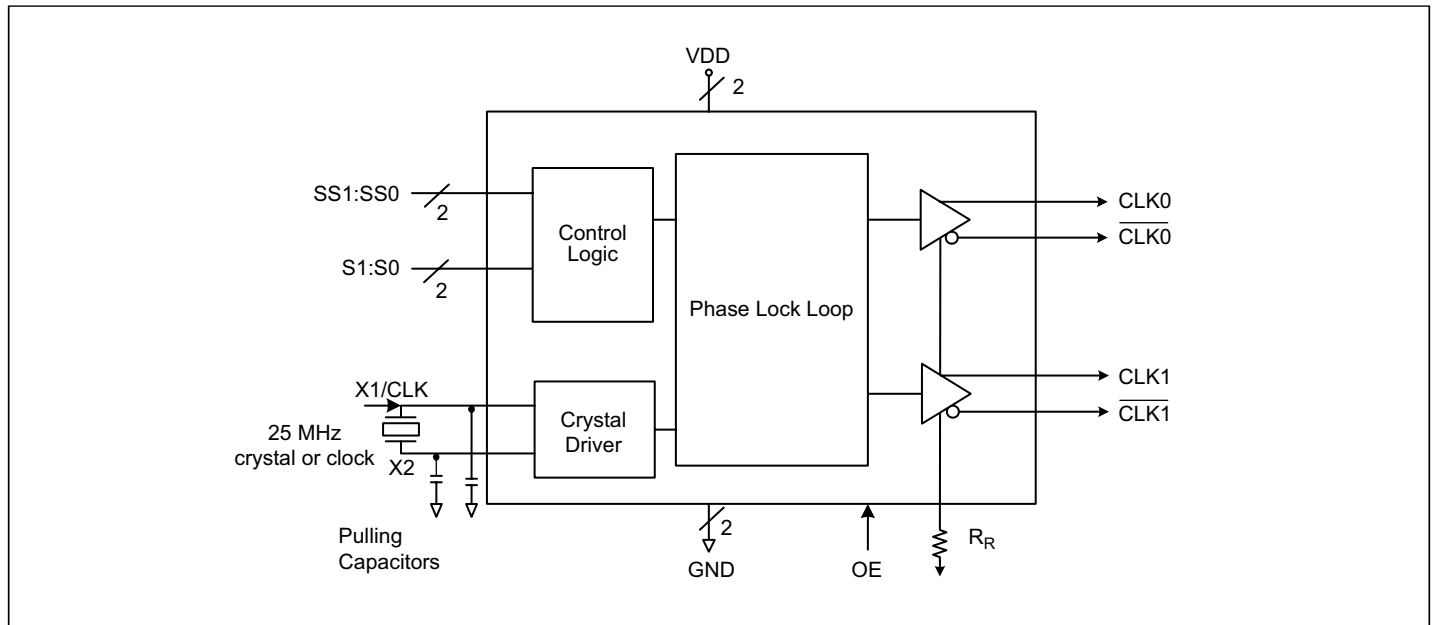
- LVDS compatible outputs
- Supply voltage of 3.3V  $\pm$ 10%
- 25MHz input frequency
- HCSL outputs, 0.7V Current mode differential pair
- Jitter 60ps cycle-to-cycle (typ)
- Spread of  $\pm$ 0.25%, -0.5%, -0.75%, and no spread
- Industrial temperature range
- Packaging: (Pb-free and Green)
  - 16-pin, 173 mils wide TSSOP

### Description

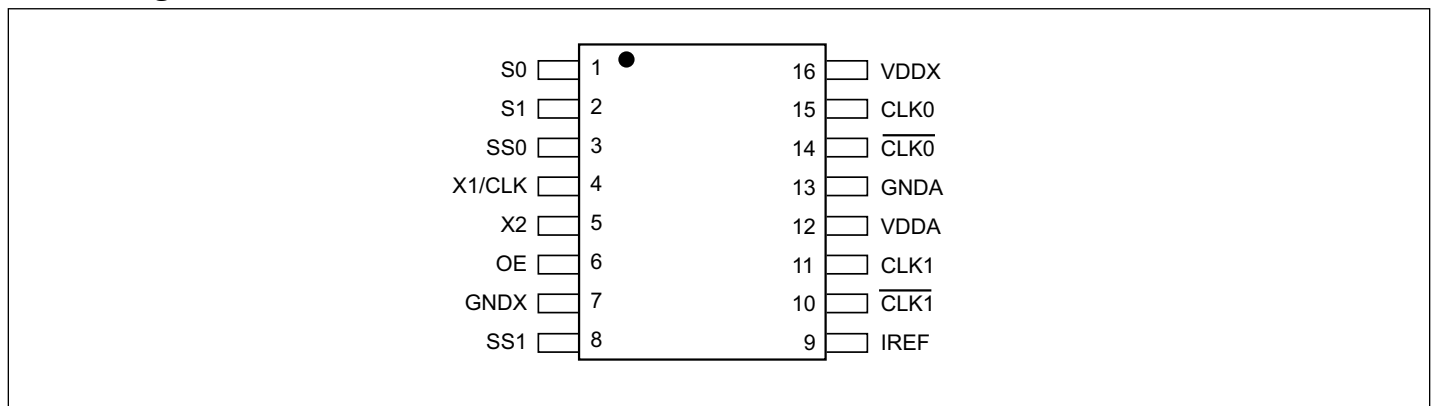
The PI6C557-03 is a spread spectrum clock generator supporting PCI Express and Ethernet requirements. The device is used for PC or embedded systems to substantially reduce Electromagnetic Interference (EMI).

The PI6C557-03 provides two differential (HCSL) spread spectrum outputs. The PI6C557-03 is configured to select spread and clock selection. Using Pericom's patented Phase-Locked Loop (PLL) techniques, the device takes a 25MHz crystal input and produces two pairs of differential outputs (HCSL) at 25MHz, 100MHz, 125MHz and 200MHz clock frequencies. It also provides spread selection of  $\pm$ 0.25%, -0.5%, -0.75%, and no spread.

### Block Diagram



### Pin Configuration



**Pin Description**

| Pin # | Pin Name                 | I/O Type | Description   |
|-------|--------------------------|----------|---|
| 1     | S0                       | Input    | Select pin 0 (Internal pull-up resistor). See Table 1.                                  |
| 2     | S1                       | Input    | Select pin 1 (Internal pull-up resistor). See Table 1.                                  |
| 3     | SS0                      | Input    | Spread Select pin 0 (Internal pull-up resistor). See Table 2.                           |
| 4     | X1/CLK                   | Input    | Crystal or clock input. Connect to a 25MHz crystal or single ended clock.               |
| 5     | X2                       | Output   | Crystal connection. Leave unconnected for clock input.                                  |
| 6     | OE                       | Input    | Output enable. Internal pull-up resistor.   |
| 7     | GNDX                     | Power    | Crystal ground pin.   |
| 8     | SS1                      | Input    | Spread Select pin 1 (Internal pull-up resistor). See Table 2.                           |
| 9     | IREF                     | Output   | Precision resistor attached to this pin is connected to the internal current reference. |
| 10    | $\overline{\text{CLK1}}$ | Output   | HCSL compliment clock output  |
| 11    | CLK1                     | Output   | HCSL clock output   |
| 12    | VDDA                     | Power    | Connect to a +3.3V source.  |
| 13    | GND A                    | Power    | Output and analog circuit ground.   |
| 14    | $\overline{\text{CLK0}}$ | Output   | HCSL compliment clock output  |
| 15    | CLK0                     | Output   | HCSL clock output   |
| 16    | VDDX                     | Power    | Connect to a +3.3V source.  |

**Table 1: Output Select Table**

| S1 | S0 | CLK(MHz) |
|----|----|----------|
| 0  | 0  | 25       |
| 0  | 1  | 100      |
| 1  | 0  | 125      |
| 1  | 1  | 200      |

**Table 2: Spread Selection Table**

| SS1 | SS0 | Spread            |
|-----|-----|-------------------|
| 0   | 0   | Center $\pm 0.25$ |
| 0   | 1   | Down -0.5         |
| 1   | 0   | Down -0.75        |
| 1   | 1   | No Spread         |

**Application Information**

**Decoupling Capacitors**

Decoupling capacitors of 0.01µF should be connected between each V<sub>DD</sub> pin and the ground plane and placed as close to the V<sub>DD</sub> pin as possible.

**Crystal**

Use a 25MHz fundamental mode parallel resonant crystal with less than 300PPM of error across temperature.

**Crystal Capacitors**

$C_L$  = Crystals's load capacitance in pF

Crystal Capacitors (pF) =  $(C_L - 8) * 2$

For example, for a crystal with 16pF load caps, the external effective crystal cap would be 16 pF.  $(16-8)*2=16$ .

**Current Source (Iref) Reference Resistor - R<sub>R</sub>**

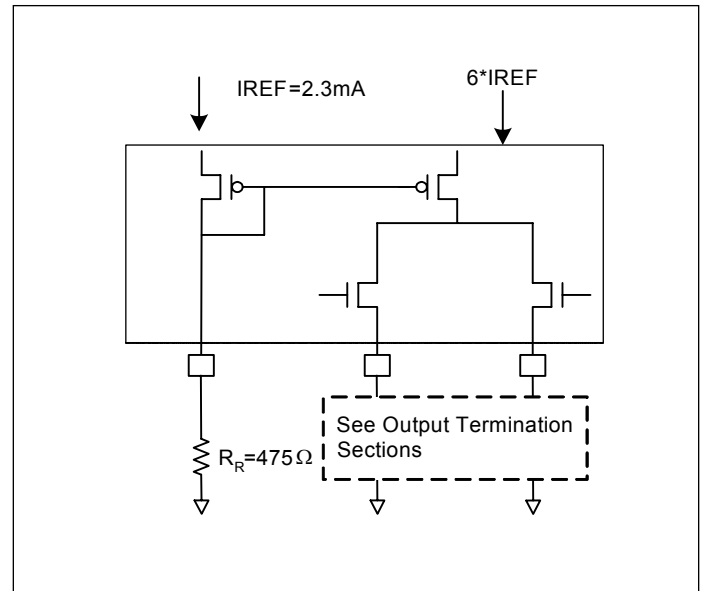
If board target trace impedance is 50Ω, then R<sub>R</sub> = 475Ω providing an IREF of 2.32 mA. The output current (I<sub>OH</sub>) is 6\*IREF.

**Output Termination**

The PCI Express differential clock outputs of the PI6C557-03 are open source drivers and require an external series resistor and a resistor to ground. These resistor values and their allowable locations are shown in detail in the PCI Express Layout Guidelines section.

The PI6C557-03 can be configured for LVDS compatible voltage levels. See the LVDS Compatible Layout Guidelines section.

**Output Structures**



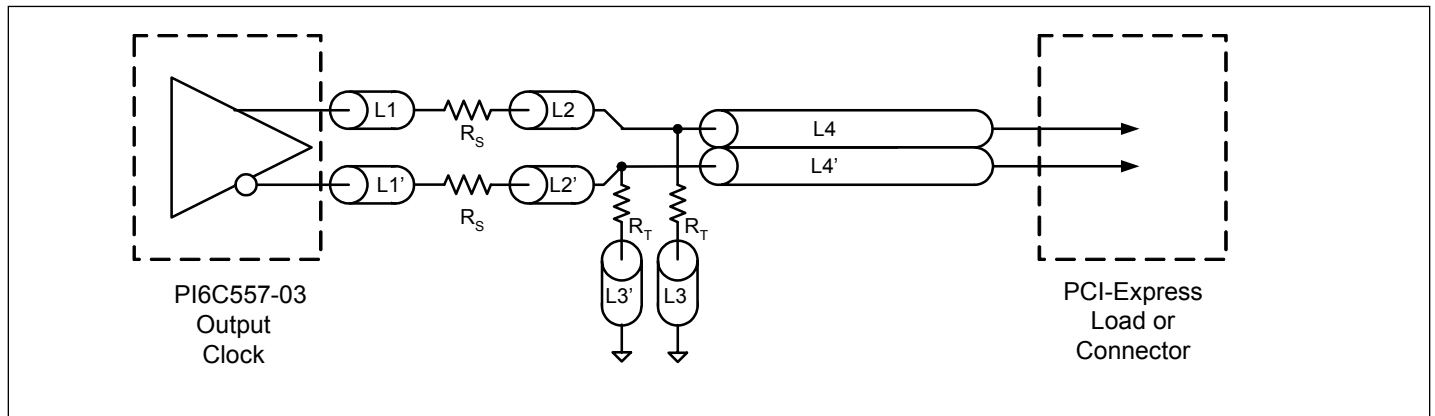
**PCI Express Layout Guidelines**

| Common Recommendations for Differential Routing | Dimension or Value | Unit |
|---|--------------------|------|
| L1 length, route as non-coupled 50Ω trace.      | 0.5 max            | inch |
| L2 length, route as non-coupled 50Ω trace.      | 0.2 max            | inch |
| L3 length, route as non-coupled 50Ω trace.      | 0.2 max            | inch |
| R <sub>S</sub>                                  | 33                 | Ω    |
| R <sub>T</sub>                                  | 49.9               | Ω    |

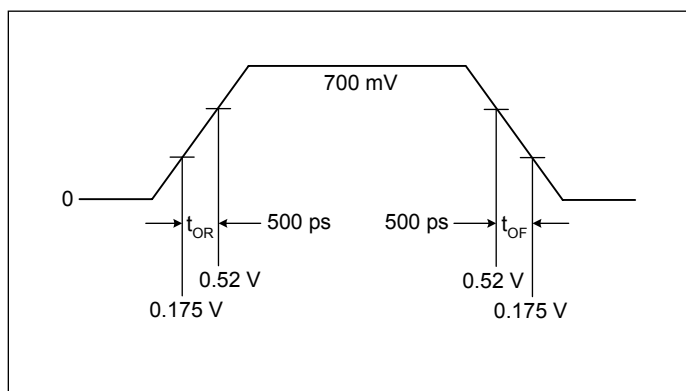
| Differential Routing on a Single PCB                            | Dimension or Value  | Unit |
|---|---------------------|------|
| L4 length, route as coupled microstrip 100Ω differential trace. | 2 min to 16 max     | inch |
| L4 length, route as coupled stripline 100Ω differential trace.  | 1.8 min to 14.4 max | inch |

| Differential Routing to a PCI Express connector                 | Dimension or Value    | Unit |
|---|-----------------------|------|
| L4 length, route as coupled microstrip 100Ω differential trace. | 0.25 min to 14 max    | inch |
| L4 length, route as coupled stripline 100Ω differential trace.  | 0.225 min to 12.6 max | inch |

**PCI Express Device Routing**



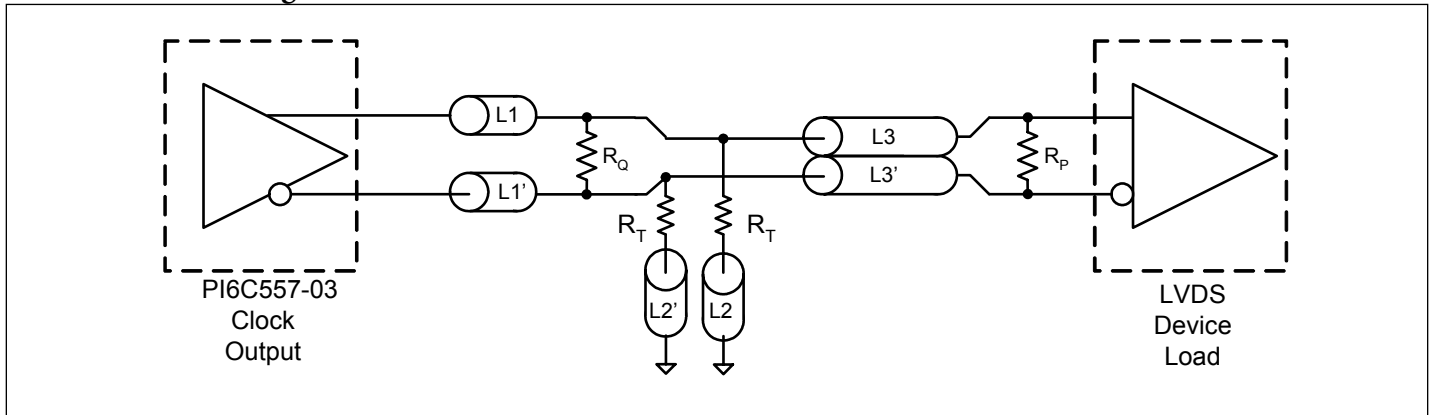
**Typical PCI Express (HCSL) Waveform**



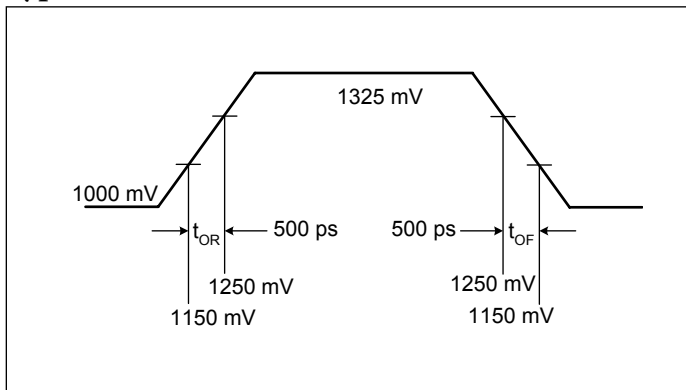
**Application Information**

| LVDS Recommendations for Differential Routing | Dimension or Value | Unit |
|---|--------------------|------|
| L1 length, route as non-coupled 50Ω trace.    | 0.5 max            | inch |
| L2 length, route as non-coupled 50Ω trace.    | 0.2 max            | inch |
| R <sub>P</sub>                                | 100                | Ω    |
| R <sub>Q</sub>                                | 100                | Ω    |
| R <sub>T</sub>                                | 150                | Ω    |
| L3 length, route as 100Ω differential trace.  |                    |      |
| L3 length, route as 100Ω differential trace.  |                    |      |

**LVDS Device Routing**



**Typical LVDS Waveform**



## Electrical Specifications

### Maximum Ratings

|   |                        |
|---|------------------------|
| Supply Voltage to Ground Potential..... | 5.5V                   |
| All Inputs and Outputs .....            | -0.5V to $V_{DD}+0.5V$ |
| Ambient Operating Temperature.....      | -40 to +85°C           |
| Storage Temperature.....                | -65 to +150°C          |
| Junction Temperature .....              | 150°C                  |
| Soldering Temperature .....             | 260°C                  |

**Note:**

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

### Recommended Operation Conditions

| Parameter   | Min. | Typ. | Max. | Unit |
|---|------|------|------|------|
| Ambient Operating Temperature                     | -40  |      | +85  | °C   |
| Power Supply Voltage (measured in respect to GND) | +3.0 |      | +3.6 | V    |

### DC Characteristics ( $V_{DD} = 3.3V \pm 10\%$ , $T_A = -40^\circ C$ to $+85^\circ C$ )

| Symbol     | Parameter                         | Conditions                     | Min.                                 | Typ. | Max.           | Unit       |
|------------|-----------------------------------|--------------------------------|--------------------------------------|------|----------------|------------|
| $V_{DD}$   | Supply Voltage                    |                                | 3.0                                  | 3.3  | 3.60           | V          |
| $V_{IH}$   | Input High Voltage <sup>(1)</sup> | S0, S1, OE, CLK, SS0, SS1      | 2.0                                  |      | $V_{DD} + 0.3$ | V          |
| $V_{IL}$   | Input Low Voltage <sup>(1)</sup>  | S0, S1, OE, CLK, SS0, SS1      | GND -0.3                             |      | 0.8            | V          |
| $I_{IL}$   | Input Leakage Current             | $0 < V_{in} < V_{DD}$          | With input pull-up and pull-downs    | -20  | 20             | $\mu A$    |
|            |                                   |                                | Without input pull-up and pull-downs | -5   | 5              |            |
| $I_{DD}$   | Operating Supply Current          | $R_L = 50\Omega$ , $C_L = 2pF$ |                                      |      | 65             | mA         |
| $I_{DDOE}$ |                                   | OE = LOW                       |                                      |      | 35             | mA         |
| $C_{IN}$   | Input Capacitance                 | Input pin capacitance          |                                      |      | 7              | pF         |
| $C_{OUT}$  | Output Capacitance                | Output pin capacitance         |                                      |      | 6              | pF         |
| $L_{PIN}$  | Pin Inductance                    |                                |                                      |      | 5              | nH         |
| $R_{OUT}$  | Output Resistance                 | CLK Outputs                    | 3.0                                  |      |                | k $\Omega$ |

**Notes:**

1. Single edge is monotonic when transitioning through region.

**AC Characteristics ( $V_{DD} = 3.3V \pm 10\%$ ,  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ )**

| Symbol                | Parameter                                 | Conditions               | Min. | Typ. | Max. | Unit    |
|-----------------------|---|--------------------------|------|------|------|---------|
| $F_{IN}$              | Input Frequency                           |                          |      | 25   |      | MHz     |
| $V_{OUT}$             | Output Frequency                          |                          | 25   |      | 200  | MHz     |
| $V_{OH}$              | Output High Voltage <sup>(1,2)</sup>      | @ $V_{DD} = 3.3V$        | 660  | 700  | 850  | mV      |
| $V_{OL}$              | Output Low Voltage <sup>(1,2)</sup>       |                          | -150 | 0    |      | mV      |
| $V_{CPA}$             | Crossing Point Voltage <sup>(1,2)</sup>   | Absolute                 | 250  | 350  | 550  | mV      |
| $V_{CN}$              | Crossing Point Voltage <sup>(1,2,4)</sup> | Variation over all edges |      |      | 140  | mV      |
| $J_{CC}$              | Jitter, Cycle-to-Cycle <sup>(1,3)</sup>   |                          |      | 60   | 100  | ps      |
| MF                    | Modulation Frequency                      | Spread Spectrum          | 30   | 31.5 | 33   | kHz     |
| $t_{OR}$              | Rise Time <sup>(1,2)</sup>                | From 0.175V to 0.525V    | 175  | 332  | 700  | ps      |
| $t_{OF}$              | Fall Time <sup>(1,2)</sup>                | From 0.525V to 0.175V    | 175  | 344  | 700  | ps      |
| $\Delta T_R/\Delta T$ | Rise/Fall Time Variation <sup>(1,2)</sup> |                          |      |      | 125  | ps      |
| $T_{SKEW}$            | Skew between outputs                      | $V_{DD}/2$               |      |      | 50   | ps      |
| $T_{DUTY-CYCLE}$      | Duty Cycle <sup>(1,3)</sup>               |                          | 45   |      | 55   | %       |
| $T_{OE}$              | Output Enable Time <sup>(5)</sup>         | All outputs              |      | 0.1  |      | $\mu s$ |
| $T_{OT}$              | Output Disable Time <sup>(5)</sup>        | All outputs              |      | 0.1  |      | $\mu s$ |
| $t_{STABLE}$          | From power-up to $V_{DD}=3.3V$            |                          | 1.6  | 3.0  |      | ms      |
| $t_{SPREAD}$          | Setting period after spread change        |                          |      | 3.0  |      | ms      |

**Notes:**

1.  $R_L = 50\Omega$  with  $C_L = 2$  pF and  $R_R = 475\Omega$
2. Single-ended waveform
3. Differential waveform
4. Measured at the crossing point
5. CLK pins are tri-stated when OE is LOW

**Thermal Characteristics**

| Symbol        | Parameter                              | Conditions | Min. | Typ. | Max. | Unit          |
|---------------|--|------------|------|------|------|---------------|
| $\theta_{JA}$ | Thermal Resistance Junction to Ambient | Still air  |      |      | 90   | $^{\circ}C/W$ |
| $\theta_{JC}$ | Thermal Resistance Junction to Case    |            |      |      | 24   | $^{\circ}C/W$ |

**Recommended Crystal Specification**

Pericom recommends:

- a) GC2500003 XTAL 49S/SMD(4.0 mm), 25M,  $CL=18pF$ , +/-30ppm  
[http://www.pericom.com/pdf/datasheets/se/GC\\_GF.pdf](http://www.pericom.com/pdf/datasheets/se/GC_GF.pdf)
- b) FY2500081, SMD 5x3.2(4P), 25M,  $CL=18pF$ , +/-30ppm  
[http://www.pericom.com/pdf/datasheets/se/FY\\_F9.pdf](http://www.pericom.com/pdf/datasheets/se/FY_F9.pdf)
- c) FL2500047, SMD 3.2x2.5(4P), 25M,  $CL=18pF$ , +/-20ppm  
<http://www.pericom.com/pdf/datasheets/se/FL.pdf>

**Packaging Mechanical: 20-contact TQFN (ZD)**

|   |  |
|---|--|
| <p>The drawing shows three views of the package: a top view, a side view, and a detail view of the lead. The top view shows a square body with 16 pins on each side. Dimensions include a body width of .169 to .177 inches (4.3 to 4.5 mm), a pin pitch of .0193 to .0201 inches (4.9 to 5.1 mm), and a lead length of .047 inches maximum (1.20 mm). The side view shows a height of .002 to .006 inches (0.05 to 0.15 mm) and a lead thickness of .004 to .008 inches (0.09 to 0.20 mm). The detail view shows a lead width of .0256 inches (0.65 mm) BSC and a lead thickness of .007 to .012 inches (0.19 to 0.30 mm). A seating plane is indicated for the lead attachment.</p> | <p>DOCUMENT CONTROL NO.<br/>PD - 1310</p> <hr/> <p>REVISION: E<br/>DATE: 03/09/05</p>                              |
| <p><b>Note:</b></p> <ol style="list-style-type: none"> <li>1. Package Outline Exclusive of Mold Flash and Metal Burr</li> <li>2. Controlling dimensions in millimeters</li> <li>3. Ref: JEDEC MO-153F/AB</li> </ol>   | <p><b>PERICOM</b><sup>®</sup><br/>Pericom Semiconductor Corporation<br/>3545 N. 1st Street, San Jose, CA 95134</p> |
| <p><b>DESCRIPTION:</b> 16-Pin, 173-Mil Wide, TSSOP</p>  |  |
| <p><b>PACKAGE CODE:</b> L</p>   |  |

Note: For latest package info, please check: <http://www.pericom.com/products/packaging/mechanicals.php>

**Ordering Information(1-3)**

| Ordering Code | Package Code | PackageType                   |
|---------------|--------------|-------------------------------|
| PI6C557-03LE  | L            | Pb-free & Green, 16-Pin TSSOP |

**Note:**

1. Thermal characteristics and package top marking information can be found at <http://www.pericom.com/packaging/>
2. E = lead-free and green packaging
3. Adding an X suffix = tape/reel